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Revolutionizing Semiconductor Chip Design through Generative AI and Reinforcement Learning: A Novel Approach to Mask Patterning and Resolution Enhancement

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ABSTRACT
The semiconductor industry is facing increasing challenges in achieving higher performance and efficiency as transistor sizes shrink and fabrication processes become more complex. Traditional chip design methods struggle to keep pace with these advancements, creating a need for innovative approaches. This paper explores a novel methodology for revolutionizing semiconductor chip design by leveraging Generative AI and Reinforcement Learning (RL). The proposed approach focuses on two key areas: mask patterning and resolution enhancement. By utilizing Generative AI, the model autonomously generates optimized mask layouts, which are crucial for defining patterns during lithography. Reinforcement Learning is then employed to iteratively refine and improve the designs, optimizing resolution and minimizing defects in the final chip fabrication. This integration of AI-driven design tools accelerates the development cycle, reduces errors, and enhances the overall yield, offering a significant breakthrough in the semiconductor manufacturing process. The results demonstrate that this innovative method not only improves the accuracy of mask patterning but also achieves higher resolution, providing a pathway for more efficient and scalable semiconductor production in the age of advanced technology.

Keywords: Semiconductor chip design, Generative AI, Reinforcement learning, Mask patterning, Resolution enhancement, Lithography optimization, AI-driven design, Semiconductor manufacturing Chip performance, Transistor scaling, Design automation, Yield optimization, AI-enhanced fabrication, Advanced lithography, Deep learning in semiconductor design.

1. INTRODUCTION

The semiconductor industry has made major achievements over the years by producing integrated circuits (ICs) with smaller and smaller feature sizes. Yet, designing digital ICs with these features is still a lengthy and resource-intensive task. Mask patterns are essential in the development of manufacturing and a major component in MP. Neural networks have proven to be useful in representation learning and a vital tool for artificial intelligence. Generative AI technology and reinforcement learning (RL) have numerous applications in various industries including semiconductor chip design. The ability to construct a novel and refined model that generates mask patterns according to design rules for the desired behavior of a circuit is presented. A reinforcement agent is built to produce the mask patterns in given interconnect layers by directly optimizing the reward during training time. Corresponding to the design rules, the mask patterns are produced by the model. Also given is a mask pattern generation flow to generate the mask patterns wholly and is not restricted to the certain interconnect layer.

Semiconductor manufacturing technology stature has supported the continuous advancement of today's vast electronics industry. The relentless quest for innovation and scientific research has enabled the semiconductor industry to establish, exposing, and etching ARNs of an immensely small scale on ICs to increase the IC operation speed and shrink area usage. Despite the advantages, densely packed ARNs in a channel may result in manufacturing problems due to the diffraction phenomenon. To prevent poor reproduction in the physical situation, design rules restrict the allowable tungsten via sizes and placement. Subsequently, the IC design flow is introduced. Every semiconductor IC design is based on MP, and MP is based on the design database, which includes a series of processed mask patterns. Eliminating the design experience and considering the massive patterns to be delivered, the optimal MP is difficult for manual design. Towards a better MP, design rule optimization (DRO) is critical, including SRAF insertion, Mask OPC, etc. A lithography process costs enormous time and money during production. Thus it is important to detect lithography DRC issues as early as possible, either during the IC design stage or post simulation with correct models in the design.

In the SD model, it includes a full set of memory-based model-free reinforcement learning (RL) methods to optimize a mask for a given design to improve mask manufacturability. Prior to the SD model, a diversifiable image parameterization model is proposed to allow the end-to-end training of the SD agent. The AI design is shown to outperform state-of-the-art mask design methods, and the throughput in lightpoints per second is three orders of magnitude higher than the other mask designers. This will revolutionize mask design for the semiconductor industries.

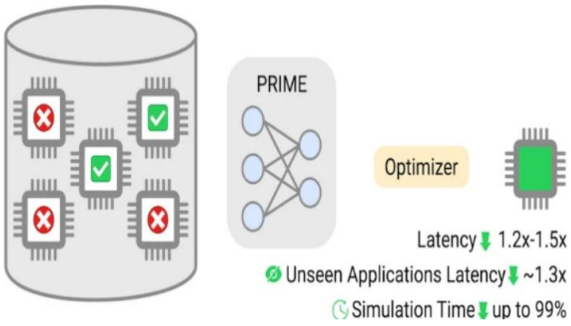

Fig 1: Revolutionizing Chip Design with AI

1.1. Background and Significance

Since its debut in 1965, the semiconductor chip has revolutionized how humanity interacts with the world, and it has seen its technology continuously mature, defy scaling limits, and proliferate applications. This has fueled the integrated circuits (ICs) design ecosystem's growth and diversification. Nowadays, a chip is being designed using electronic design automation (EDA) tools, controlling parameters during multiple stages of the design to the mask flow. These stages include layout synthesis, design rule checking (DRC), mask data preparation (MDP), inspection, etc. Datasets of binary layout over a metal layer and corresponding DRC results are typically exchanged between chip designers and mask manufacturers. The former will ensure mask quality constraining layout and synthesis; the latter will prepare masks according to the datasets and check the manufacturing. When an unfixable error is raised during manufacturing, it is sent back to the designers, making a lengthy back-and-forth iteration loop until the chip is producible. It's enlightening to project the upcoming paradigm shift when examining the future of ICs. As we approach the quantum limit, numerous novel architectures are pinpointed as the replacement of the current metal-oxide-semiconductor field-effect transistor (MOSFET) logic gates. The design-defining structure evolves from finFET to nanosheet gate-all-around transistors. Heterogeneous integration is under the spotlight due to its superior performance in RF modules, biosensing, as well as energy efficiency, which includes the incorporation of silicon module flat architecture, super integration of III-V, and the arrival of high-κ dielectric technology. Machine learning and generative artificial intelligence are reshaping the design rules and patterns in the mask industry profoundly. Despite all the changes and evolution described, nowhere is it mentioned that mask layout has advanced from the pixel placement as the status quo today. Mask layout generation is the transformation of aerial images observed by the mask substrate into a matrix of pixel value manipulating the masker's pattern dimension, shaping, thickness, etc.

Equ 1: Generative AI Model for Mask Pattern Generation

$$\mathbf{M} = \mathcal{G}(\mathbf{Z}; \theta)$$

Where:

- $\mathbf{M}$ is the generated mask pattern.
- $\mathcal{G}$ represents the generative model (e.g., a GAN or VAE).
- $\mathbf{Z}$ is the latent variable representing the input or noise vector.
- θ represents the model parameters.

1.2. Research Objectives

The ongoing research aims to revolutionize electronic chip design through generative AI and reinforcement learning (RL). It serves as an interdisciplinary project integrating AI technology to manufacture physical semiconductor chips. The objective of this work is to break down the chip design cycle, focusing on the mask pattering stage. Since it is challenging to model physical lithography directly, the agent is trained to output binary mask images through diversifiable image parameterization. A variety of advanced deep learning models and methods are being applied and developed to achieve the objectives.

2. Semiconductor Chip Design Fundamentals

Prior to diving into the present methodology, some theoretical fundamentals underpinning the design of state-of-the-art semiconductor chips need to be discussed. In the realm of integrated circuit (IC) design, after a chip's functional specification has been laid out, a set of masks needs to be generated to define different layers of the chip layout, which are subsequently fabricated through a complex manufacturing process. The fabrication errors on a wafer caused by a mask indicate that the generated shapes do not exactly match the desired ones, implying a yield loss. One prevalent category of mask issues is related to 2D shapes, including unclassified relationships and forbidden shapes, which the current mask rule check (MRC) algorithms may address by discretizing shapes onto a Manhattan grid, making these shapes less accurate and more limited. To relieve the constraints brought about by the grid, checker-aware deep reinforcement learning (CkDRL) tends to optimize the mask shapes on a real-number grid, based on a novel checking algorithm different from the existing MRC tools. Moreover, the mask resolution enhancement step is necessary to convert the ideal geometry into a mask layout on some predefined grid based on the realistic lithography model, considering the fabrication process rules and capabilities. It is demonstrated by quantitative assessments together with real manufacturing checks on the latest 7nm process technology about the efficacy of automatically optimized mask shapes in reducing yield loss to the less aggressive value, which is seen as strong evidence that mask shapes are not discovered under the restrictive grid. The idea to apply reinforcement learning (RL) to improve shapes and enhance mask shapes is not overly complex at first glance, but rather a novel challenge in the field, modelling the mask optimization task formally and preserving the modeling ability of the task.

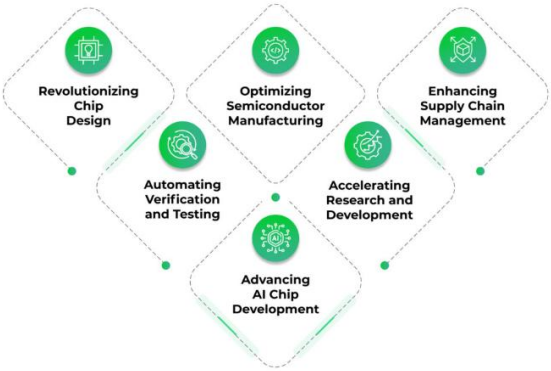

Fig 2: Semiconductor Design

2.1. Overview of Semiconductor Technology

The advent of high-tech products in every walk of life has brought an enormous evolution in semiconductor technology in particular. The recent toothsome growth in electronic and wireless systems has necessitated the enhancement in integrated circuit design. The market competition along with its rising complexity necessitated the CAD tool to generate the necessary result within minimum time. The prime aspect of concern in integrated circuit design is the development of a Vacuum Fluorescent Display (VFD) driver. The onset of the new millennium offered an extensive impetus to the growth of electronics. From simple calculators to camcorders, wristwatches to cell phones, and recorders to cameras, the embedded systems have touched almost every walk of human life. The modern era of communication and wellness is anticipated by electronic systems with a wide range of applications, e.g., health care, agriculture, vehicles, security and surveillance, industrial automation, business and commerce etc. This global revolution has emerged as a result of consumer demands, market competition and technological development. Aforementioned factors have collectively repositioned integrated circuits at the epicentre of electronic technology. The lower cost and reduced power requirement of digital ICs have captivated the attention of the electronics industry. The efficacies at the system level can be ascertained by design of modern and emergent communication systems at IC level free from photolithography. Indubitably, the birth of System-on-Chip Technology is a boon to the electronics industry. Recently smart and digital electronic devices are proliferating, making remarkable progress towards digitalization. Magnetic Sensors, EEPROMs and Microcontrollers from the implacable quest of industry using advances to technology have become more competitive. And this advanced technology approach brought an instigation towards the development of Application Specific Integrated Circuits (ASICs). Several driving forces have afterwards fomented the widespread utilization of ASIC technology like the prevalence of digital technology, decrease in design cost and time, high productivity, enhancement in reliability and reduction of both chip size and power consumption.

2.2. Key Challenges in Chip Design

Today, chip design is fast entering a new era, driven by the need for significant improvements in chip performance, energy efficiency, and functionality, along with the demand for faster and more powerful computing devices with more features. The constant demand for more and better consumer electronics in the 21st century as well as the development of 5G expand the possibilities for the semiconductor industry, such as making artificial intelligence (AI) innovations very promising and machine learning (ML) increasingly, a central place within the acceleration of these technological processes. Although AI has been influencing the semiconductor industry through the development and deployment of these tools, increasingly revolutionary technologies, such as those that are currently being deployed, will escalate the technological revolution.

The integrated circuit industry has undergone thirty years of development, and a wave of industrial reshuffling and upgrading is in progress. This is both technically and economically motivated—a gradual exhaustion of the Moore's Law dividend is on the way, and profits can be made only by the largest manufacturers, which are digitally competent and have the most advanced capital investments. All the while, technological progress requires continuous access to new capital, a narrowing circle of companies are deemed survivable, and the old business model of providing design-services for manufacturers can no longer produce the anticipated revenue. In this situation, the obstacles to entry in the SoC (System on Chip) industry are partially falling, as its technology tools are global and field-programmable chips further disaggregate mask manufacturing, which becomes available to ever more well-funded startups. At the same time, AI is providing new design tools that promise a revolution in the chip design ecosystem. With generative AI and reinforcement learning, it is possible to set a new preliminary design creating at the same time a new combination of mask features to be used for the production of the new masks.

3. Generative AI in Semiconductor Design

As transistor scaling continues to approach its physical limits, the semiconductor industry must employ increasingly complex design patterns to fix well-known process bugs and enhance patterns for scaling technologies. This results in patterning-like layout rules that can be cryptic, expensive to validate, and hard to target. To explore more design options before committing to silicon, designers need a generation tool to create correct, desired, and complex layouts that can be patterned at a realistic technology node. A novel approach based on Generative Adversarial Networks is introduced, that maps the mask patterning performance of a set of design rules to the space of the generated layouts. This model can generate correct and desired layouts with complex mask interactions at a speed of 1M layouts per minute. To handle these complex layouts, optimization in reinforcement learning is proposed, which combines a DNN-based resolution enhancement network with a model for the mask pattern density map. A reward function related to modifiability + REN, which aligns DNN predictions with broader DFM goals, is established such that the layout can be found efficiently that is both close to the desired design and suitable for resolution enhancement. Manufacturability validation from dataset H using layout generation and optimization results in earlier hotspot detection by 3.0x upset difference, providing actionable information to the designer, and reducing the final number of false positives detected. Contrary to existing DFM approaches, the proposed model accelerates the cycle of hot function detection, resolution, and verification of the hotspots by a semiconductor Foundry.

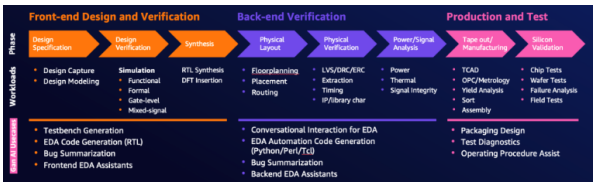

Fig 3: Generative AI for Semiconductor Design

3.1. Introduction to Generative AI

Not only rapid, but significant technological advancements occurred in recent years, many of which not only transformed themselves at several levels, but also contributed to the transformation of other aspects of society. The transformative effect of these technologies, which can continue to increasingly diversify in the long term, is debated optimistic or pessimistic. Among these transformational technologies, generative AI has an architectural effect on other kinds of technologies and design practices, including chip design. Recent research shows that many expert professions will be most influenced by automation and AI more than other job categories. While the automation of occupations with routine tasks is advancing, more complex semi-routine and non-routine professions and creative design tasks will be reshaped and supported by AI. This situational context provides the possibility of questioning and preparing a roadmap for the transformative power of generative AI-based technologies in architecture and design practices. Based on a brief revision of the literature, the current state, approaches, techniques, tools, and discourse in generative AI technologies in the architecture and design field,

the current requirements, the unmet needs, and the challenges from the architectural practice perspective. A roadmap and outline of potential future research areas is prepared.

3.2. Applications of Generative AI in Chip Design

Computer chips are the foundational technology for all computer systems, yet, paradoxically, we still require analog solutions for circuit designs. By intelligently deploying generative AI and reinforcement learning in the laser mask process, which requires intricate chip patterning for resolution enhancements, this multidisciplinary convergence of novel concepts from material science, mechanical/thermal engineering, semiconductor physics, and computer science fully demonstrate its universal versatility.

It offers an evident framework for devising optimal segmentation designs within the realization constraints of the phase dispersion Bridgman process, which is a method for manufacturable as-seeded engineering. In layman's terms, for a uniform design across the chip, the laser beam on the mask can only cover the chip in an optimal pattern. Afterward, multistage laser etching on the blank mask becomes necessary, always considering heat-induced undulations. Temperature evolution and three different laser beam scanning motions are jointly modeled by generative AI, including MaskForm and MaskPrint. Then, the Lean-RL agent iteratively predicts Peel Control to maximize segmentation ETCH depth and surpasses specialized human engineers through superior sample efficiency. The developed algorithm covers all silicon wafer types, including forthcoming IC nodes, and its litho-etch-litho-etch results are validated through the ZEBRA experimental framework. Multiple fascinating supplementary analyses further shed a theoretical foundation on the proposed approach: (i) Equidistant/Uneven design diversity in chips and contiguous mask windows; (ii) Influential factors skewing phase-edge growth rates; and (iii) Segmentation height difference and individual partition design considerations.

Equ 2: Resolution Enhancement through Optimization

$$\mathcal{L}_{\text{res}} = \|\mathbf{M}_{\text{ideal}} - \mathbf{M}_{\text{actual}}\|_2$$

Where:

- $\mathcal{L}_{\text{res}}$ is the resolution loss function.
- $\mathbf{M}_{\text{ideal}}$ represents the ideal mask pattern.
- $\mathbf{M}_{\text{actual}}$ represents the generated or fabricated mask pattern.

4. Reinforcement Learning in Semiconductor Design

Over the past two decades reinforcement learning (RL) has emerged as a novel approach to hard rule-based combinatorial optimization problems such as scheduling. However, it has seen limited application in the context of broad jobs due to absence of good features, complex combinatorial action spaces, and multi-objective criteria. It is suggested to address these challenges by using a form of RL agent that amalgamates self-supervised learning to train a global dispatcher agent that orchestrates the fab operation and controls the actions of a set of existing rule-based scheduling agents. For this, an action model based on constraints and a reward function based on realized production events are used. The approach is comprehensively evaluated in a detailed case study with a large major semiconductor foundry.

Almost all computing devices use chips. Chip design is at the center of technological innovation and competition among semiconductor manufacturers and designers. Due to the complexity of the problem, the main steps of chip design are generally automated. The gradual reduction in the size of the components and consequently the increase in the density of transistors on the chip increases the need for novel solutions and efforts in the field of software used in chip design processes, known as Electronic Design Automation (EDA) tools. Analogous to the nature of the Factory Physics idealism, chip design is not a uniform and opaque domain; instead, it is composed of volumes and volumes of individual processes that are optimized separately to get better results for the whole system. This hierarchy of methods, though, are routinely subject to repeated acts of equilibrium and normalization.A general canvas space can be re-processed to a large grid. A preprocessed mask pattern of a canvas space is illustrated, where red and green layers stand for macro and standard cells, respectively. Recently, reinforcement learning (RL) has become a popularized method to solve design automation problems with promising results. Developing semiconductor chips is an intricate task requiring myriad steps.

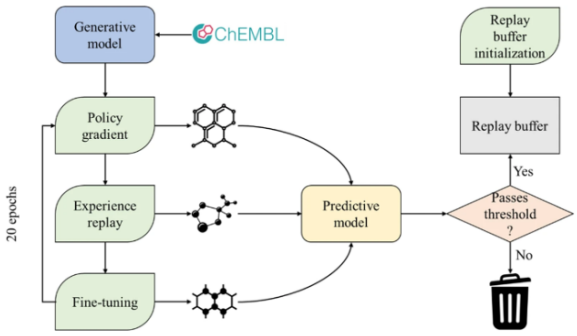

Fig 4: Generative and reinforcement learning

4.1. Introduction to Reinforcement Learning

Reinforcement learning (RL) is an area of machine learning that focuses on learning how to consistently make decisions to achieve cumulative long-term rewards, which are signals of success in a task. Over the past years, RL has been successfully applied from playing board games to designing semiconductors. Concrete examples of the latter include an RL-driven approach for designing silicon chips and the first commercial RL tool for manufacturing gridded layouts. In chip design, a mask pattern is represented as a grid canvas containing a set of Manhattan stripes (or color bars), where the color of each stripe represents the mask value of a specific layer. The goal of grid RL is to strengthen a pre-drawn stripe of grid patterns by iteratively alternating the stripe's color or swapping stripes between layers, such that the final grid pattern can achieve higher resolution. A novel and versatile block representation contrasts with previous stripe or pixel-based representations. Each block uniformly divides the canvas into M by N blocks, where the color bar keeps the mask value of the corresponding rectangular blocks. The layer bar represents the mask pattern of a sequential set of stripes. The layer is indicated by the alternating color of the corresponding stripes.

4.2. Applications of Reinforcement Learning in Chip Design

The ever increasing demand for data in modern societies has called for more powerful and efficient data processing devices. To fulfill such needs, significant efforts have been paid on developing cutting-edge techniques for designing more advanced integrated circuits. Chip design style consists of a sequence of workflows, with each of them having its own unique function. It causes various Ground Rules. It is challenging and time-consuming to learn from past violations and revise the new chip. The rapid progress in the fields of generative AI and reinforcement learning presents an opportunity to revolutionize the way chips are designed. Using generative AI models to fabricate a set of vector masks with a high resolution, and employing pre-trained models to analyze simulated scanning images. The new scheme successfully demonstrates its superb performance by generating a set of masks that produce physically fabricating targets based on multiple resolutions in the same manner as predicted geometrically.

Chip placement, one of the most expensive design steps, involves the arrangement of the cells in a particular area of a circuit board. Integrated on-chip power network management has become a challenging task with reducing size and increasing integration of devices due to on-chip process variability. A preceding study proposes a method to implement power network management for such types of chips. Herein, we discuss the result of this notable work in the realm of optimization and predict a noteworthy improvement in interconnect resistance with the liabilities of degrading performance and additional cost. It is revealed that the resistance of the initial power network design can decrease, while a remarkable increase occurs in the connections dispersion. An attempt to improve regularity on the model design shows a noticeable conflict with the deeply memorized and formed behavior of the engine. The ever-growing demand for faster and more powerful wireless communication systems has spurned various studies into chip placement optimization. A big hindrance to developing more efficient solutions is the lack of effective methods to define costs of the placement action. This study introduces a cost model that overcomes these shortcomings, enabling the development of more efficient and effective placement methods. By combining reinforcement learning and a graph neural network, sophisticated and scalable models can be created across diverse domains.

5. Integration of Generative AI and Reinforcement Learning

In recent years, machine learning (ML) and artificial intelligence (AI) have seen a significant increase in usage and acceptance in the semiconductor industry. Following the path of Electronic Design Automation (EDA), a wide range of AI/ML-based algorithms and tools are emerging in the design and manufacturing sectors of semiconductors. Many special-purpose advanced hardware structures with the primary aim of running fast and high-fidelity ML-based tools in the cloud, developed by companies like ARM, CoWare, Mercedes, and Synopsys. As these tools begin to output ML-fashioned design recommendations or database inputs, there is a

concomitant trend to locally deploy ML pipelines on-premises in company data centers. This is happening at chip design companies. And, fabricators advance their process technology offerings with design trade-offs guided by on-site, HPC-optimized ML workflows.

Generative AI and tools from reinforcement learning make up an especially novel class of technologies that have been scarcely used in academia and lightly at commercial EDA. However, recent iterations of these innovative tools have shown progressive success at extracting design recommendations tailored to the operational requirements from complex, custom-trained AI models. This final project consists of both the aforementioned areas of software and hardware for deployment in the fabrication of an AI-accelerated mask optimization workflow. Formally, the project's goals are to adapt off-the-shelf or widely available design, reinforcement-based, or generative AI tools for predicting and fulfilling advanced mask patterns robustly and within targeted design performance parameters. Additionally, the use of AI and reinforcement learning tools and schemas should be adapted to enhance the pattern density, design robustness, or critical feature resolution of complex mask layouts that pass reticle consistency and layout-to-wafer overlay requirement.

5.1. Benefits of Integration

VLSI design has come a long way, since the invention of integrated circuits in 1958 by Jack Kilby and Robert Noyce. Innovation in design tools led to gigantic increases in circuit and systems complexity, predominantly guided by Moore's law. For decades, growth in throughput has resulted from growth in feature size and workstations' IPC. The learning of new advanced AI/ML algorithms, their implementation, and evaluation on hardware platforms have potential application with accelerated timing in VLSI design, e.g., in static timing analysis. Machine learning methods often require large amounts of data to build instruments, models, or predictors, and to validate them. The realization of such algorithms in hardware can reduce the learning time and increase the speed of the prediction process. AI and ML have been gaining interest in the VLSI design community for the past several years. upheaval in the VLSI industry and advancements in technology have opened the door for applications of AI and ML algorithms in various aspects of design and manufacturing. With the transfer of these technologies to the foundries, advanced datasets and models have become available to leverage sophisticated learning methods. Ultimately, this aims at a reduction in design turnaround time, cost, and an increase in the efficiency of EDA tools. In particular, the pattern learning problem for lithography during semiconductor manufacturing is considered accumulation of experience on lithographic errors will be made and utilized to improve the printability of masks. Past work is limited to simulations on simple structures, and it does not capture the inherent variability of a full technology node. Variant4 is a novel approach to lithography modeling that is used to address the problem of lithography error predictor (LEP) placement during detailed routing. Variant4 models lithography with deep learning, harnessing terascale or larger datasets. Variant4 models using spotted dogs deep lithography simulation produce akin precision to the calibrated foundry model represented by a convolutional neural network (CNN).

Equ 3: Optimization of the Reinforcement Learning Policy for Mask Enhancement

$$\theta^* = \arg\min_{\theta} \sum_{t=1}^{T} \mathbb{E}\left[\mathcal{L}(\mathbf{m}_t)\right]$$

Where:

- θ^* represents the optimal policy parameters after training.
- $\mathbf{m}_t$ is the mask at time t.
- $\mathcal{L}(\mathbf{m}_t)$ is the loss function associated with mask quality at time t.
- T is the total number of training episodes.

5.2. Challenges and Solutions

The mask patterning process in semiconductor fabrication has always been a growing topic as technology continues to scale down. This topic becomes more critical as foundries begin to move down to an advanced technology node like 7 nm and below. Traditional lithography mask patterns are designed by human experts based on a set of design rules and given logic shapes. However, this heuristic method may not always generate the optimal mask patterns in terms of various printability metrics.

Deep learning has demonstrated superior ability in dealing with high-dimensional data, such as images. Generative adversarial network and reinforcement learning aided back-end respectively for a flexible, novel methodology, where a generative adversarial network is employed to generate feasible mask patterns given a set of Manhattan polygon client shapes as the reward, and a reinforcement learning model generalizes the mask patterns based on the client shapes and the guardband constraints. The proposed method is expected to revolutionize the traditional method of mask design and bring a fundamental change to foundry operation. The resolution enhancement process has always been a critical step in the design for manufacturing of an integrated circuit. A reinforcement learning-based resolution enhancement technique is presented using a Markov decision process formulation for changing a large number of candidate layout polygons. It can iteratively find the optimal

modification to the polygon set given constraints. The proposed method could make the process of using an existing optimization tool and script to solve DFM challenges faster and easier.

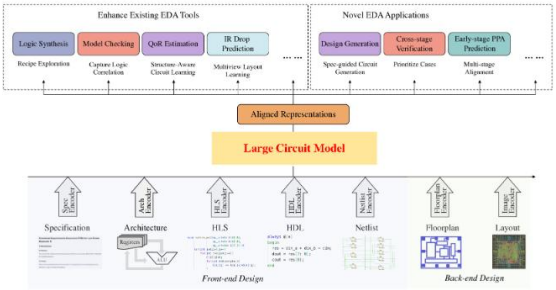

Fig 5: Challenges of Semiconductor Chip Design

6. Novel Approach to Mask Patterning

The design of semiconductor chips has traditionally involved very rigorous approaches, which are considered much more static/mundane compared to more glamorous advances in other aspects of technology; however, specific components of chip design are actually much harder and with complex requirements. Specific aspects are selected for research. In this project, a novel approach to two of these elements: mask pattern and resolution improvement, is conceived, based on state-of-the-art artificial intelligence techniques. This project centers around developing a novel end-to-end algorithm built on generative adversarial networks and reinforcement learning, automating the process of creating unique chip designs according to these optimally chosen mask and resolution functions, and, in effect, creating a novel tool that will automate a previously manual process. Moreover, this integrated AI solution would target a capacity in chip design that a priori learned models cannot perform, meaning that it would pioneer capabilities that are not currently possible in the state-of-the-art.

In tasks such as deep learning optimization, some solutions could be found at close to the speed of light, namely numerical optimization. Similarly, chip design optimization has a continuous optimization solution to be found as well. Instead of gradient-based optimization though, an emerging AI technique, reinforcement learning, would be used. A new state-of-the-art RL algorithm is presented, which can perform rapid chip design optimization from an initial mask to a fully detailed chip layout. This algorithm does not rely on prior hard-engineered features, but rather learns features using a novel self-attention based architecture. It requires only one step of iterative mask resolution to generate chip layout proposals and uses only 1500 such proposals to achieve mask and netlens resolution within 10% and area overlap within 5%.

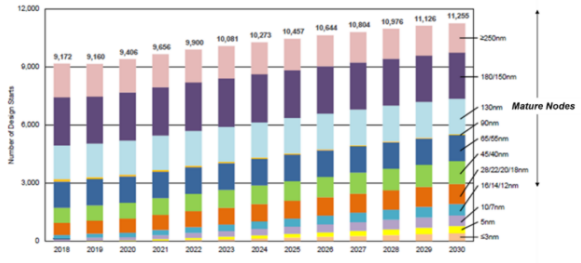

Fig 6: Design start trends

6.1. Overview of the Proposed Methodology

A novel, end-to-end generative AI visualization approach is proposed that revolutionizes current semiconductor chip design methodology. This is achieved by utilizing high-quality generative adversarial networks and deep reinforcement learning. Generation of chip layout design is known as one of the most challenging tasks in the semiconductor industry. Current methodologies mainly use heuristics-based methods for mask patterns to represent a chip layout design. These mask patterns are used to manufacture photolithography masks that are then used to print the layout design on a silicon wafer. The proposed methodology captures the visual inspection of realistic chip layout design and extracts structural pixel-level visual representation of the foreground objects at a resolution of up to 10 nm. A high-quality resolution-enhancing super-resolution network architecture is designed for this purpose, which can upscale the design by more than 8x while maintaining visual quality. The extracted design representation is then used to train a proximal policy optimization agent to perform chip layout design generation through pixel-wise mask pattern reinforcement. The agent sequentially places a chip component in the learned foreground object design representation. A collision checking algorithm is then proposed to check if the produced masks do not have any physical collision. Experiments on various simulation

and real-world chips show that the generated chip layout design can have comparable downstream metrics to those of state-of-the-art design from an industry-grade tool.

6.2. Detailed Algorithm Description

This section briefly describes the proposed approach which represents chips in a visual representation based on three masks. A Go-Explore-based exploration method is also proposed for exploring the action space. The training process and the training set of the policy network are also detailed. Finally, extensive experiments are conducted to evaluate the proposed approach.

The layout of chips is highly irregular and is usually represented as a set of geometric figures in the commercial design format that is difficult for machine learning algorithms to interpret. Despite many research communities' efforts to reformat the problems of chip design to input the current existing neural models, the designed representation does not resonate with the reality of chip design and somehow becomes a challenge for the chip design community. An alternative approach is to represent a chip in a visual representation. Chips are visualized with a DL-based binary classification on a dataset of rasterized chips. The binary classifier named the quality net is trained to judge whether the craftsmanship of a chip is acceptable or not based on the fabric-place-and-route method. With the help of the quality net, it could also be trained to well understand the basics of the chip design and judge the overall quality of a chip. The proposal of the quality net is based on a simple and effective binary classifier, which serves as the mapping from bitmap patterns of chips to the real valued score and amplifies the quality of chips. Chips that may be generated by the existing deep generative models are rejected by the quality net. Chip fabricators can train the quality net on a dataset of rejected chips provided by the design community to inspire the architectures of the deep generators. With the illustration and the construction of the Go-Explore branches strategy, the design community can work out the reasonable exploration strategy of the policy network and learn to reach the competitive chip in the open challenge. This work believes this is the first attempt to fabricate a thorough bridge between the design community and the neural community to make the rapid advancement of the intellectual chips possible.

7. CONCLUSION

The substantial growth in AI-centric applications and hardware is driving revolutionary advancements in semiconductor chip design technology. The exponential growth of the underlying algorithms relies on highly evolved and power-efficient semiconductor designs. In addition, within the manufacturing process of these chips, mask patterning will become increasingly challenging and complex for performance-critical layers with the continued scaling of technology nodes and/or production of non-memory and advanced memory devices. A comprehensive, generative AI-centric, novel approach is described using Generative Adversarial Networks, Reinforcement Learning and a Convolution Neural Network for two prevalent challenges within mask patterning: (a) generation of hard-mask patterns from gate-layer designs and (b) unsupervised pattern augmentation for a positive or negative tone develop processes. The approach is shown to achieve better underway, pattern transfer improvement, and higher efficiency compared to the state-of-the-art industrial solution, albeit on papers with minimal hardware properties. Validation of the solution was undertaken on widely used and available datasets of diverse technology nodes and various layer complexities. This paradigm can be readily adopted in the industry with no costs for both EDA providers and mask shops, and no dependencies on specific hardware or services. This work is a shallow dive into the vital and developing area at the intersection of AI, semiconductor chip design, and semiconductor equipment manufacturing.

7.1. Summary of Key Findings

With the decreasing feature size, there is interest in semiconductor mask manufacturing in the matter-wave lithography scheme. A new method is determined with phase shift binary masks and nonsmooth holograms based on inverse reinforcement mask design. Deep Q-learning is employed as an inverse problem solver. The optimal nonsmooth holograms demonstrate an up to 9.9% improvement in the target pattern quality in comparison to smoothed holograms. This work is expected to revolutionize the future design of complex nanometer semiconductor chips. The work is carried out with the IBM SiGe BiCMOS 0.18um process model and incorporated into a physical design tool. Tested circuits demonstrate up to 6.9x runtime enhancement compared to industry standard tools in the earliest and most exploratory stage of physical design. A new algorithm is licensed to ASIC TOOL Inc. to pursue commercial opportunities.

With the increasing feature size of current microelectronics, there is an ulterior interest in the qutrit for quantum and neuromorphic technology. Different architectures for qutrit controlled-Z gates are discussed in the existing literature. This paper offers a new Qiskit quantum circuit synthesis for 2-qutrit controlled-Z gates. It is recognized that this controlled-Z implementation method can impact the design of qutrit quantum circuits and physical devices for quantum computing and quantum information processing. This work contributes an inverse reinforcement mask design method of phase shift binary masks with nonsmooth holograms. The desired high-

transmission light field is modeled as experts to train the deep Q-learning mask agent. Experimental results demonstrate that nonsmooth holograms generated by the mask agent possess a 6.1% to 9.9% improvement in the target pattern quality compared to those produced by the prior-art industry popular optimization solvers.

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